Fig. 1A

ASK 100%
Modified Miller, 106kbit/s

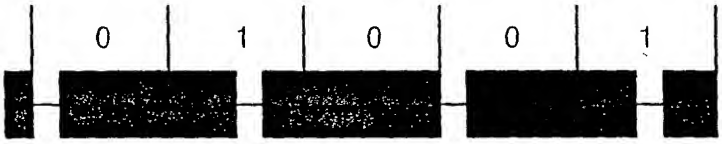


Fig. 1B

Load Modulation
Subcarrier f/16
OOK
Manchester,106kbit/s

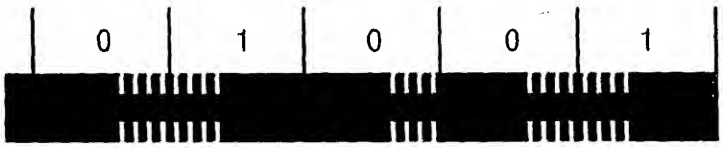
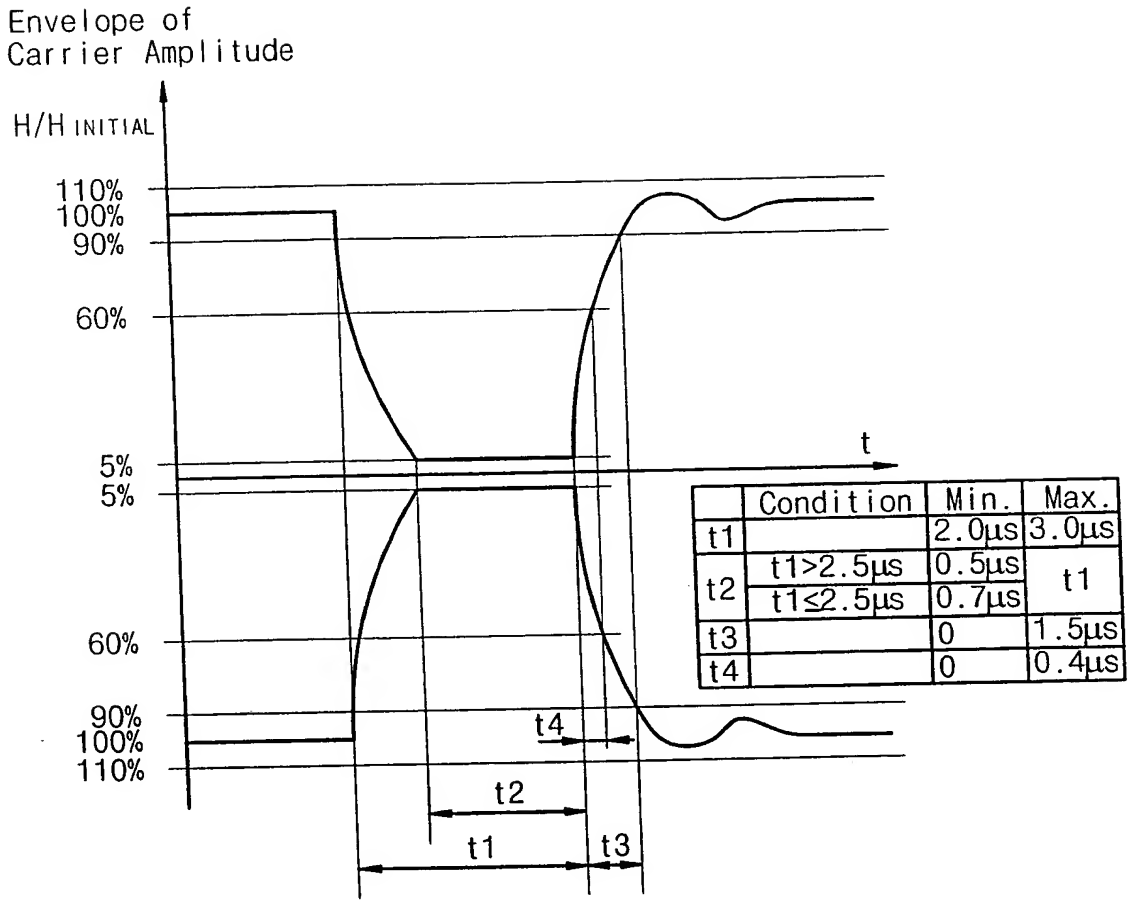


Fig. 2



	Condition	Min.	Max.
t1		2.0μs	3.0μs
t2	t1>2.5μs	0.5μs	t1
	t1≤2.5μs	0.7μs	
t3		0	1.5μs
t4		0	0.4μs

Fig. 3A

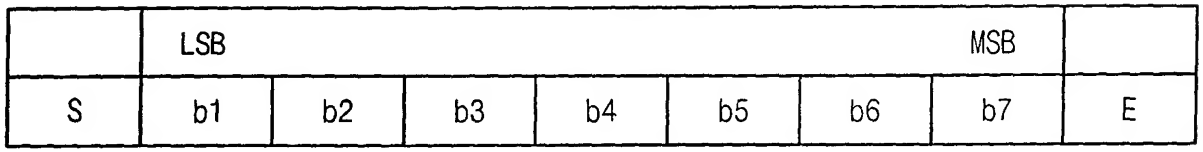

LSB
MSB
S
b1
b2
b3
b4
b5
b6
b7
E

Fig. 3B

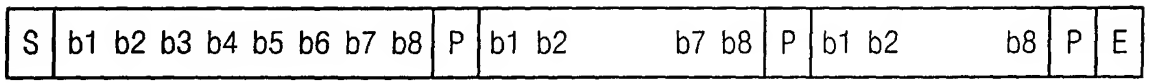

S
b1 b2 b3 b4 b5 b6 b7 b8
P
b1 b2
b7 b8
P
b1 b2
b8
P
E

Fig. 4

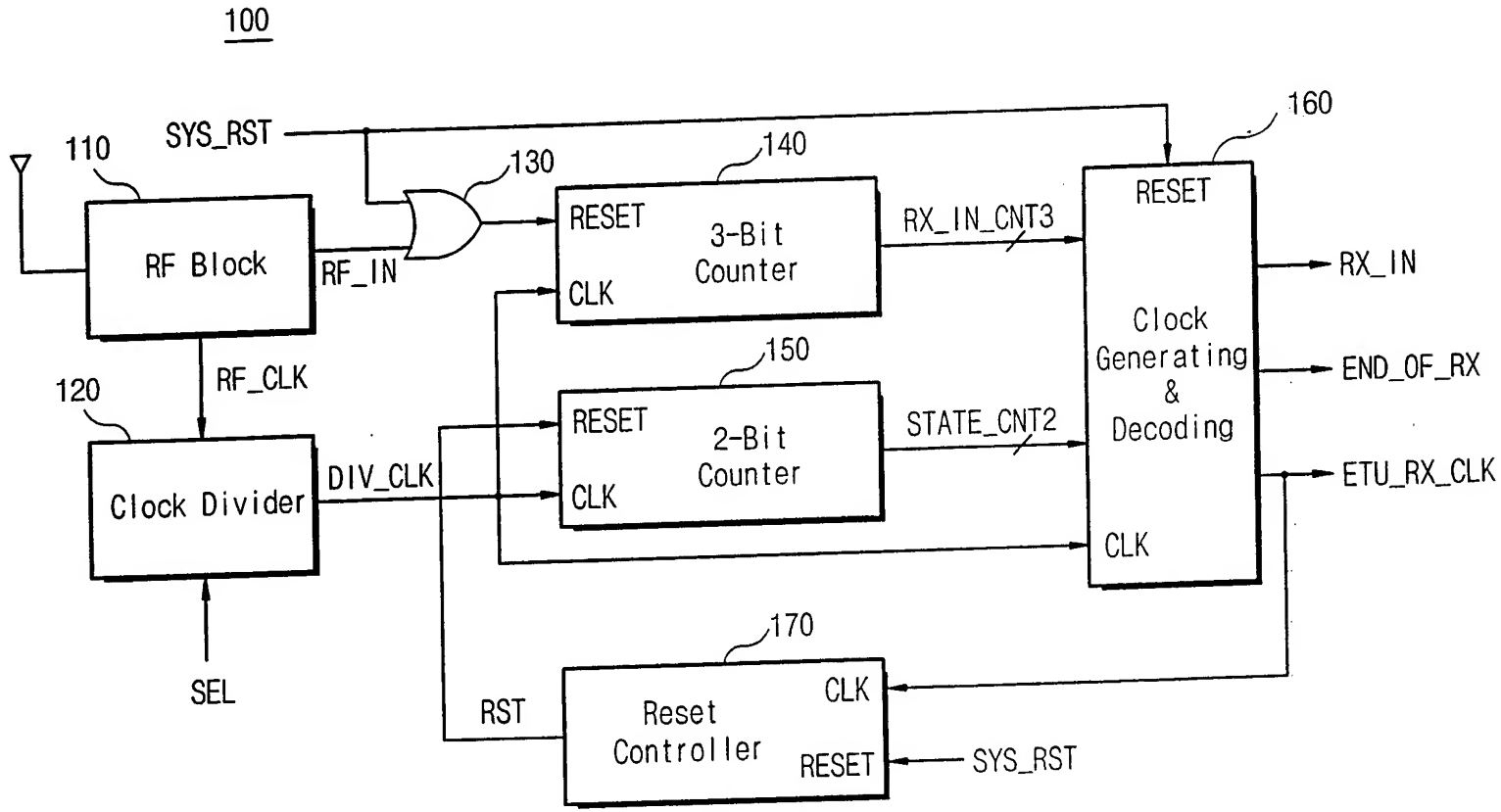

100
110
SYS_RST
130
140
160
RF Block
RF_IN
RESET
3-Bit
Counter
CLK
RX_IN_CNT3
RESET
RX_IN
Clock
Generating
&
Decoding
END_OF_RX
ETU_RX_CLK
CLK
RF_CLK
120
150
RESET
2-Bit
Counter
CLK
STATE_CNT2
Clock Divider
DIV_CLK
SEL
170
RST
Reset
Controller
CLK
RESET
SYS_RST

Fig. 5

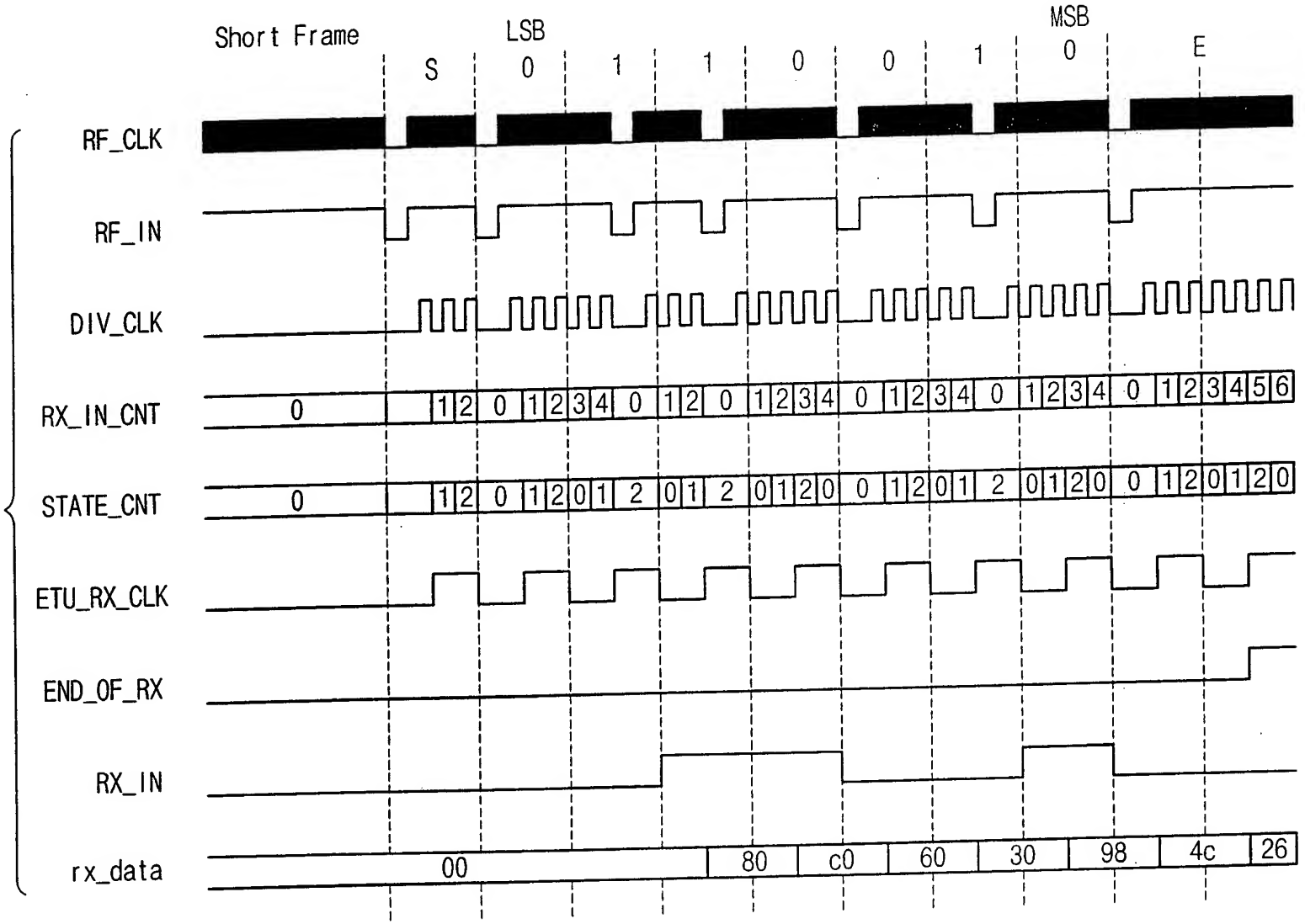

Short Frame
LSB
MSB
S
0
1
1
0
0
1
0
E
RF_CLK
RF_IN
DIV_CLK
RX_IN_CNT
STATE_CNT
ETU_RX_CLK
END_OF_RX
RX_IN
rx_data
00
80
c0
60
30
98
4c
26

Fig. 6

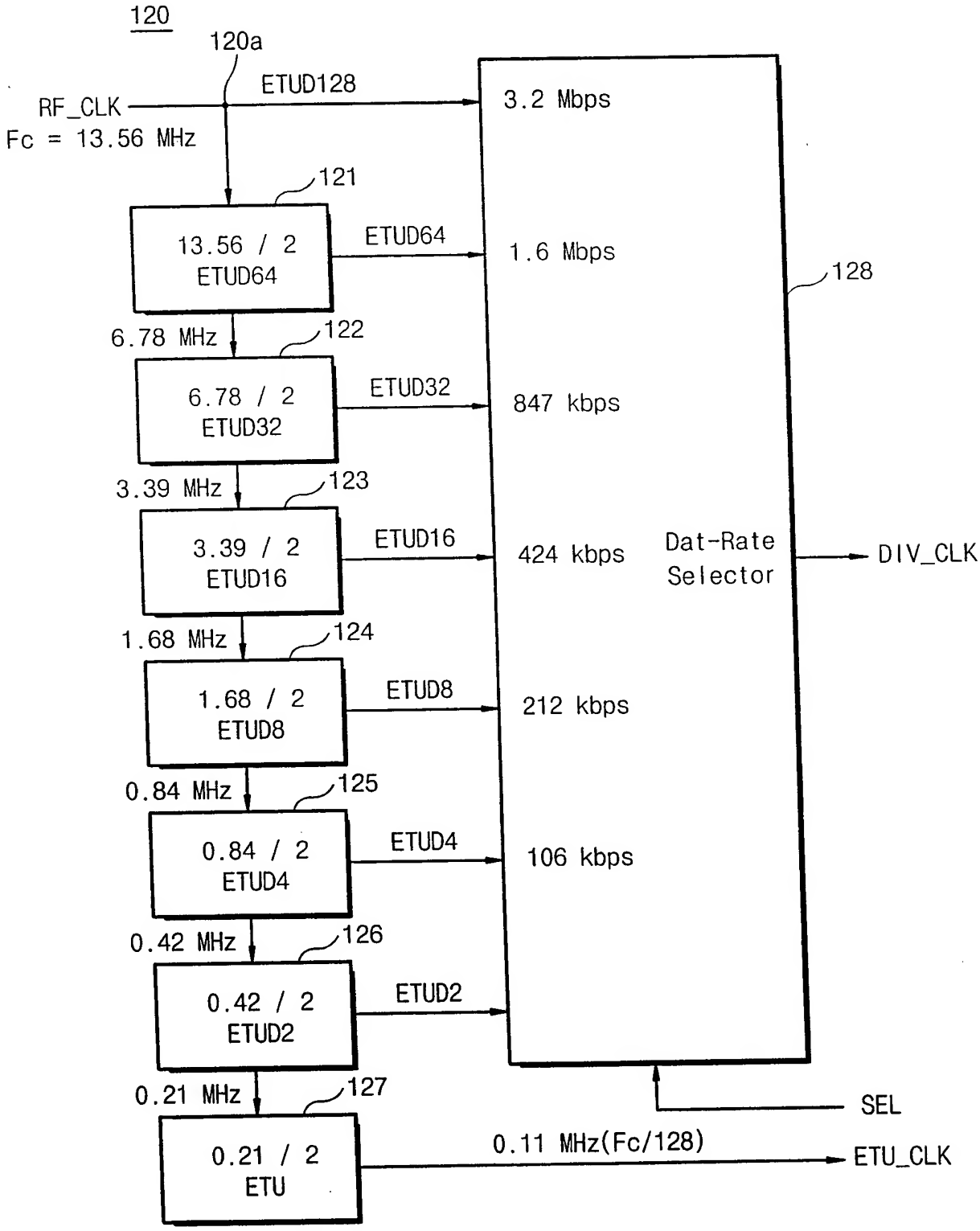

120
120a
RF_CLK
Fc = 13.56 MHz
ETUD128
3.2 Mbps
121
13.56 / 2
ETUD64
ETUD64
1.6 Mbps
128
6.78 MHz
122
6.78 / 2
ETUD32
ETUD32
847 kbps
3.39 MHz
123
3.39 / 2
ETUD16
ETUD16
424 kbps
Dat-Rate
Selector
DIV_CLK
1.68 MHz
124
1.68 / 2
ETUD8
ETUD8
212 kbps
0.84 MHz
125
0.84 / 2
ETUD4
ETUD4
106 kbps
0.42 MHz
126
0.42 / 2
ETUD2
ETUD2
0.21 MHz
127
0.21 / 2
ETU
SEL
0.11 MHz(Fc/128)
ETU_CLK

Fig. 7

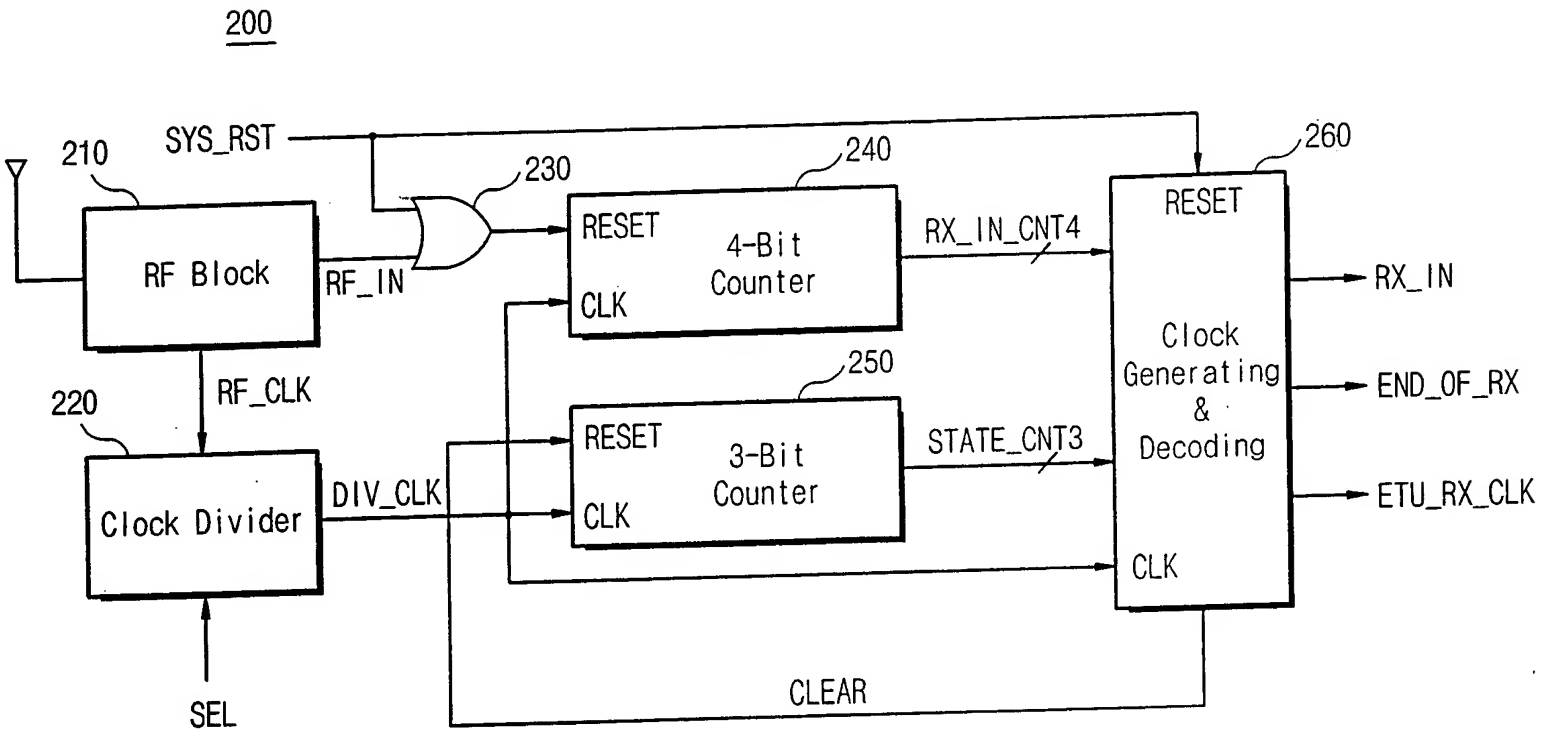
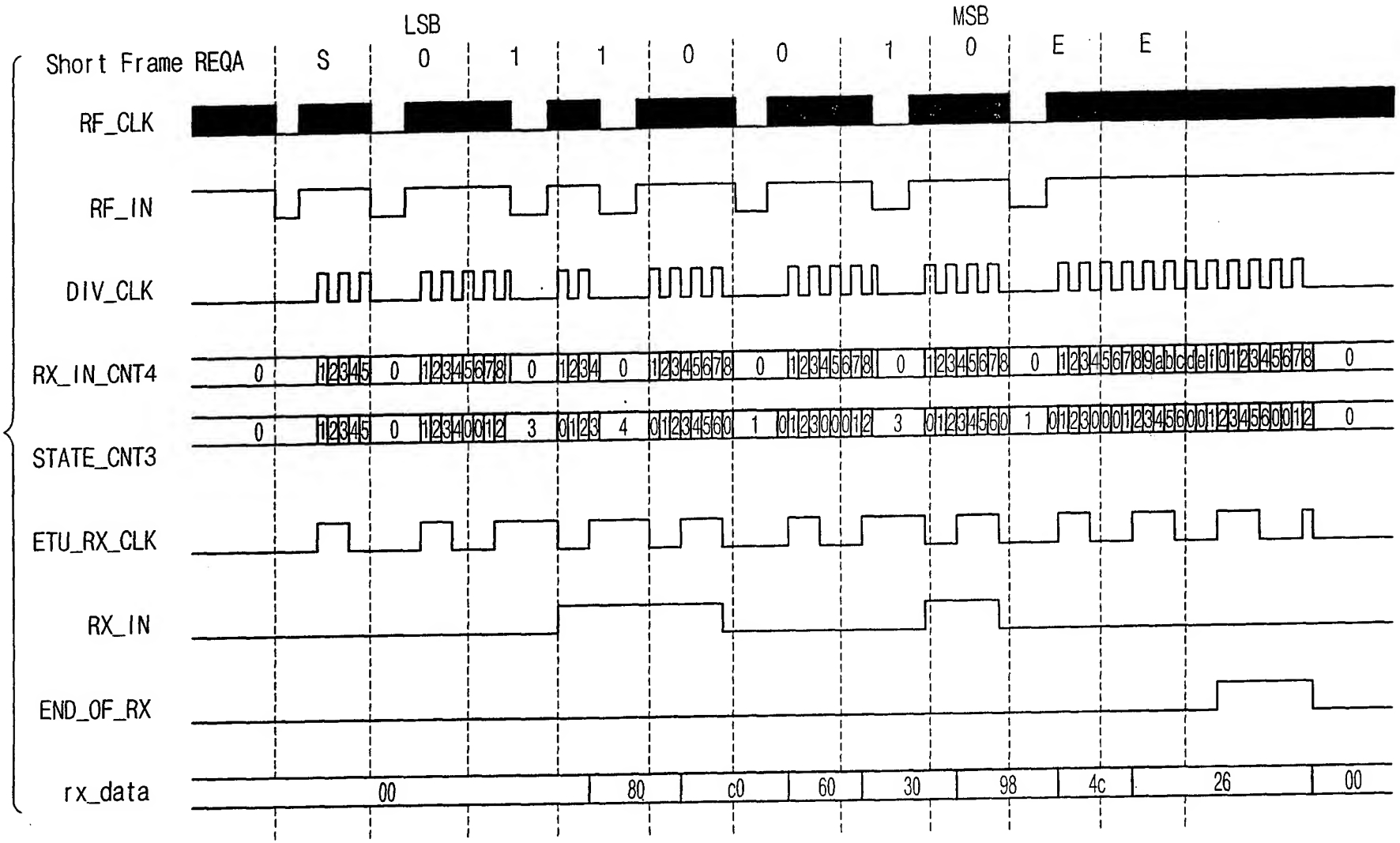

200
210
SYS_RST
230
240
260
RF Block
RF_IN
RESET
CLK
4-Bit
Counter
RX_IN_CNT4
RESET
RX_IN
RF_CLK
220
250
Clock
Generating
&
Decoding
END_OF_RX
RESET
3-Bit
Counter
STATE_CNT3
Clock Divider
DIV_CLK
CLK
ETU_RX_CLK
CLK
SEL
CLEAR

Fig. 8


LSB
MSB
Short Frame REQA
S
0
1
1
0
0
1
0
E
E
RF_CLK
RF_IN
DIV_CLK
RX_IN_CNT4
STATE_CNT3
ETU_RX_CLK
RX_IN
END_OF_RX
rx_data
00
80
c0
60
30
98
4c
26
00